Remarks

This amendment is responsive to the Office Action dated July 30, 2004. Upon entry of the amendment, claims 1-7 will be pending. Claim 5 has been amended to include the recitation of "a testing item of" to provide the antecedent basis for dependent claims 6 and 7. Marked up and Replacement Sheets have been attached herewith to correct Fig. 3 and Fig 4. In view of the foregoing amendments and the following remarks, reconsideration of the present patent application is respectfully requested.

Priority Document

An English translation of the priority document is attached herewith.

In the Office Action Summary, the Examiner indicated that only some of the certified copies of the priority documents had been received and included the note, "*See the attached detailed Office action for a list of the certified copies not received." However, the detailed Office action did not contain a list of the certified copies not received. Clarification is requested since the applicant believes that all required certified copies have already been submitted.

Objection to the Drawings

The Examiner objected to the drawings as failing to comply with 37 C.F.R. 1.84(p)(5) because they do not include the reference characters mentioned in the text. Specifically, the Examiner stated that Fig. 3 lacked reference number "331" and Fig. 4 incorrectly referred to reference numbers "41, 42, 43, 44, 46 and 47." Applicants have amended the drawings and have attached herewith copies clearly showing the amendments in red ink. Applicant has also enclosed replacement sheets with formal versions of amended Figs. 3-4 to replace original Figs. 3-4 and effectuate the amendments. Applicants respectfully request that the objections to the drawings be withdrawn.

Objection to the Specification

The Examiner has objected to the specification because specification did not refer to the appropriate parts of Fig. 4 as shown in the drawings. Applicants have amended Fig. 4

to conform to the specification. Applicants respectfully request that the objection to the specification be withdrawn.

Rejection under 35 U.S.C. §112

The Examiner rejected claims 6 and 7 under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. In particular, the Examiner stated that claims 6 and 7 lacked antecedent basis for the terms "said local product" and "said local analog product." Applicants have amended claim 5 to include the terms "a testing item of" to provide the proper antecedent basis for claims 6 and 7. This amendment is supported by the specification and figures of the present application as originally filed, and therefore there is no new matter added therein. Applicants respectfully request that the rejection under 35 U.S.C. §112, second paragraph be withdrawn.

Rejection under 35 U.S.C. §103

Claims 1-3 have been rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. patent No. 6,434,503, (hereinafter "Sommer") and further in view of U.S. patent No. 5,845,234, (hereinafter "Testa et al."). The Applicants respectfully disagree. Reconsideration of the present patent application is respectfully requested.

It is well-established that

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. **Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.**
>
> The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.

M.P.E.P. § 2143, *citation omitted, emphasis added.* Applicants respectfully submit that the combined teachings of Sommer and Testa et al. do not provide a teaching or

suggestion to establish an intellectual property including a tester library, a tester resource installation configuration and a testing strategy; integrating the intellectual property with a product target specification, an error code list and a program transfer rule check; and automatically developing a source code prototype of the testing program.

It is to be emphasized that the present invention has at least following features. (1) An **intellectual property** including a tester library, a tester resource installation configuration and a testing strategy is established. (2) At least a **tester library**, a **tester resource installation configuration**, a **testing strategy,** a **product target specification**, an **error code list** and a **program transfer rule check** are integrated. (3) A source code prototype of the testing program is automatically developed.

However, although Sommer discloses a master program for a tester, it is to be noted that the master program is a library of files and merely coordinates testing functions (Column 1 lines 13-23). Thus, the master program of Sommer can only correspond to the tester library of the present invention. Consequently, Sommer does not teach or suggest an **intellectual property** including the tester program, a **tester resource installation configuration** and a **testing strategy**, *i.e.* Sommer does not teach or suggest the intellectual property of the present invention.

With regard to the Examiner's comments in the office action that the step of integrating the intellectual property with a product target specification, an error code list and a program transfer rule check in the present invention corresponds to the "device under test 102" of Sommer, the Applicants respectfully disagree based on at least following reasons.

Referring to Fig. 1 and Column 3, lines 19-23 of Sommer, it is disclosed that the production testing for a device under test 102 is run based on the code from a production test program 100, and the production program 100 may include hundreds of files used to store and execute a test program for a semiconductor wafer tester 92. For clarity, **the "device under test 102" of Sommer is used for executing a test program for a wafer tester**." However, it is to be emphasized that the method of **the present invention is used for automatically developing a test program of a tester**. Hence, the functions of the present invention are different from those of the "device under test" of Sommer, and furthermore the "device under test 102" of Sommer is incapable of integrating an

intellectual property, a product target specification, an error code list and a program transfer rule check.

The method of the present invention provides a step of integrating the intellectual property with a product target specification, an error code list and a program transfer rule check. Furthermore, the intellectual property of the present invention includes a tester library, a tester resource installation configuration and a testing strategy. However, Sommer does not teach or suggest an intellectual property including a tester library, a tester resource installation configuration and a testing strategy. In addition, Sommer does not teach or suggest an integration of an intellectual property, a product target specification, an error code list and a program transfer rule check. Therefore, Sommer does not disclose all the elements of the present invention. Because Sommer fails to teach all the elements of the present invention, applicants respectfully submit that claim 1 is not *prima facie* obvious over Sommer.

Testa et al. discloses a system and a method for generating a testing program code. However, Testa et al. divides the translation process into two steps, wherein the first step is to translate a waveform description into a unified ATE format, and the second step is to take the unified ATE format and supply the data to completing templates of test program modules (Column 2 lines 17-24). Thus, **the means and the contents of the present invention are completely different from those of Testa et al.**

Accordingly, Testa et al. does not cure the deficiency of Sommer, namely the lack of a system wherein an intellectual property including a tester library, a tester resource installation configuration and a testing strategy, a product target specification, an error code list and a program transfer rule check are integrated to develop a source code prototype of the test program. It is to be noted that the present invention provides a novel method for automatically developing a testing program of a tester for chip design, and moreover that **the present invention simplifies the transfer among the testing procedures of different testers**.

Finally, claims 2 and 3 depend from independent claim 1. As discussed above, Sommer lacks a teaching of an intellectual property including a tester library, a tester resource installation configuration and a testing strategy, a product target specification, an error code list and a program transfer rule check are integrated to develop a source

code prototype of the test program. As also discussed above, Testa et al. does not cure the deficiencies of Sommer. Accordingly, since claim 1 of the present invention is patentable over Sommer and Testa et al., and claims 2 and 3 depend from the claim 1, dependent claims 2 and 3 are all also allowable as being dependent on the allowable claim 1. Accordingly, favorable reconsideration and withdrawal of the rejection under 35 U.S. C. § 103(a) is respectfully requested.

The Examiner has also rejected claims 4-6 under 35 U.S.C. 103(a) as being unpatentable over Sommer and Testa et al. as applied to claim 1 above and further in view of Mydill (U.S. Patent No. 6,574,760, hereinafter "Mydill"). As discussed above, Sommer does not teach or suggest integration of an intellectual property, a product target specification, an error code list and a program transfer rule check. Also as discussed above, Testa et al. does not cure the deficiencies of Sommer, namely a system wherein intellectual property including a tester library, a tester resource installation configuration and a testing strategy, a product target specification, an error code list and a program transfer rule check are integrated to develop a source code prototype of the test program

Applicant respectfully submits that Mydill also fails to cure the deficiencies of Sommer and Testa et al. While Mydill may teach an analogous testing system including parts such as: pin electronics, parametric measurement units, device power supplies and a high-speed clock, Mydill does not teach or suggest an intellectual property including a system wherein a tester library, a tester resource installation configuration and a testing strategy, a product target specification, an error code list and a program transfer rule check are integrated to develop a source code prototype of the test program. Because, Mydill does not cure the deficiencies of Sommer and Testa et al. in regards to claim 1, dependent claims 2-6 are also patentable over Mydill. Accordingly, favorable reconsideration and withdrawal of the rejection under 35 U.S. C. § 103(a) is respectfully requested.

The Examiner has rejected claim 7 under 35 U.S.C. § 103(a) as being unpatentable over Sommer, Testa and Mydill as applied to claim 5 above, and further in view of Toner (A BIST Scheme for SNR, Gain Tracking and Frequency response of a Sigma-Delta ADC, hereinafter "Toner").

Toner teaches a built-in-self test (BIST) for an on-chip measurement of SNR (signal-to-noise reduction), GT (gain tracking), and FR (frequency response) of an ADC (analogue-to-digital converter) out put response. Toner does not teach or suggest a system wherein an intellectual property including a tester library, a tester resource installation configuration and a testing strategy, a product target specification, an error code list and a program transfer rule check are integrated to develop a source code prototype of the test program, thus Toner does not cure the deficiencies of Summer, Testa et al. and/or Mydill in regards to claim 1 (or claim 5). Therefore, claim 7 is patentable over Summer, Testa et al, and Mydill in view of Toner. Accordingly, favorable reconsideration and withdrawal of the rejection under 35 U.S. C. § 103(a) is respectfully requested.

Based on the above amendments and remarks, the allowance of the present invention is respectfully requested.

Date: 10/28/2004

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"ENGLISH TRANSLATION OF PRIORITY DOCUMENT TAIWAN PATENT APPLICATION NO. 89125261 FILED ON NOVEMBER 28, 2000"

INTELLECTUAL PROPERTY AND METHOD FOR DEVELOPING TESTING PROGRAM OF TESTER

The present invention relates to an intellectual property and method for automatically developing a testing program of a tester, and more particularly to establishing a library having testing program modules for various testers so as to quickly produce a testing program for various testers, to share and to reuse the resource.

Nowadays, chips are quickly developed and designed in accordance with system on chip (SOC). Thus, the functions of chips are more powerful. However, there exist some problems, such as the complexity of testing chips, the development of testing programs, the transfer among different testers and the modification of the programs, which would increase the cost of maintenance so as to influence time to market.

Currently, many chip designs are based on system on chip, and in order to solve the above problems, it is important to utilize intellectual property (IP), in particular, chip design IP and tester IP to automatically develop source code prototype of a testing program. The present invention provides a concept that the source codes of various testers are produced in response to various testing items from the various formats of various machines formed from the same one simulation pattern, so that when the inputs of the simulation pattern, pin-define, testing items, specification conditions and machine types are prepared, the inputs are used for producing the source code of the tester and the pattern via an IP program. Accordingly, the control programs are developed faster and the program conversion can be achieved therefrom. Therefore, it is more convenient, more efficient and less costly to develop a new testing

program.

In order to overcome the foresaid conventional drawbacks, the object of the present invention is to provide an efficient production of a testing program, wherein the testing programs of the various testing machines can be switched from one another, so that the testing programs can be reused efficiently, and the test efficiency speeds time to market.

In order to achieve the foresaid object, the present invention provides an intellectual property of testers for automatically developing a testing program of a tester, comprising:

a tester library having testing program modules for plural testers, wherein the testing program modules are produced according to a testing strategy of the testers; and

an operation platform for automatically converting and producing the testing program of the tester in response to a testing requirement of the tester and according to the testing strategy of the tester library

According to the intellectual property of testers for automatically developing a testing program of a tester, the tester includes a digital tester.

According to the intellectual property of testers for automatically developing a testing program of a tester, the tester includes an analog tester.

According to the intellectual property of testers for automatically developing a testing program of a tester, the tester includes a Trillium tester, a Schlumberger ITS serier tester, an HP 9491 tester, an Advantester T7315 tester and a VTT V7100 tester.

According to the intellectual property of testers for automatically developing a testing program of a tester, the testing strategy includes a

testing item of a logic product and a testing item of an analog product.

According to the intellectual property of testers for automatically developing a testing program of a tester, the testing item of the logical product is one selected from a group consisting of continuity test, drive/sink current test, power dissipation test, IDDQ test, input leakage current test, function pattern test and AC characteristic test.

According to the intellectual property of testers for automatically developing a testing program of a tester, the testing item of the analog product is one selected from a group consisting of ADC/DAC's SNR test, THD test, Jitter/Skew test, crosstalk test, eye diagram test and frequency response test.

In addition, the present invention provides a method for automatically developing a testing program of a tester, including following steps of:

establishing a testing program module for plural testers, wherein the testing program module include a testing strategy for the plural testers; and

automatically converting and producing a source code of the testing program of the tester according to a testing requirement and the testing strategy.

The above objects and advantages of the present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description and accompanying drawings, in which:

Fig. 1 shows the tester library according to a preferred embodiment of the present invention;

Fig. 2 shows the tester resource installation configuration according to

the preferred embodiment of the present invention;

Fig. 3 shows the testing items of the testing strategy according to the preferred embodiment of the present invention; and

Fig. 4 is a view illustrating the integrated items according to the preferred embodiment of the present invention.

Reference symbols list:

11:tester library

12:Trillirum tester

13:Schlumberger ITS serier tester

14:HP 9491 tester

15:Advantester T7315 tester

16:VTT V7100 tester

21:tester resource installation configuration

22: precision electronics (PE) specification and max. channels

23: precision measurement unit (PMU) specification

24: device power supplies (DPS) specification

25: time measurement unit (TMU) specification 25

26: vector memory size specification

27: system clock rate specification

28: analog channel specification

31: testing strategy

32: extra item (analog product)

321: ADC/DAC's SNR and THD test

322: Jitter/Skew test

323: crosstalk test

324: eye diagram test

325: frequency response test

33: normally item (logic product)

331: continuity test

332: drive/sink current test

333: power dissipation test

334: IDDQ test

335: input leakage current test 336: function pattern test

337: AC characteristic test

41: test program source code prototype 42: tester library

43 tester resource installation configuration

44: program transfer rule check 45: error codes list

46: product target specification 47: testing strategy

In order to complete the IP of the present invention, each configuration of the tester source code, the definitions of C or Pascal languages and the definition of the pattern format are first illustrated in Fig. 1. Referring to Fig. 1, the tester library 11 according to a preferred embodiment of the present invention includes information of five testers, for example Trillium Tester 12, Schlumberger ITS serier Tester 13, HP 9491 Tester 14, Advantester T7315 Tester 15 and VTT V7100 Tester 16. The pattern file format and the source code prototype of testing program of each tester are provided in accordance with the user's demand. In addition, the testing programs for satisfying the same testing demand could be converted into the testing programs of other testers.

Fig. 2 shows the tester resource installation according to the preferred embodiment of the present invention. The inputting conditions of the IP are defined in accordance with the testers and the electrical specification. The testing programs and the pattern files allowed for a user will be developed according to the pre-set inputting conditions. The tester resource installation configuration 21 shown in Fig. 2 essentially includes precision electronics (PE) specification and max. channels 22, a precision measurement unit (PMU) specification 23, a device power supplies (DPS) specification 24, a time measurement unit (TMU) specification 25, a vector memory size specification 26, a system

clock rate specification 27 and an analog channel specification 28.

Fig. 3 shows a normally testing strategy of a standard logic product. The item of the testing strategy 31 includes a normally item (logic product) 33, and an extra item (analog product) 32. The normally item 33 essentially includes continuity test 331, drive/sink current test 332, power dissipation test 333, IDDQ test 334, input leakage current test 335, function pattern test 336 and AC characteristic test 337. In addition, the extra item 32 further includes ADC/DAC's SNR and THD test 321, Jitter/Skew test 322, crosstalk test 323, eye diagram test 324 and frequency response test 325.

The IP can be implemented by using C language or C Shell Script so as to integrate the foresaid data bank, and thereby the IP could be executed in a personal computer (PC) or a workstation so as to increase speed of development of the testing programs as shown in Fig. 4. Software components of various testers are installed in the IP and compatible with one another, so that the programs can be increased or modified among different testers only by changing the associated programs to achieve simple and fast modification. Please refer to Fig. 4, the test program source code prototype 41 are formed by the tester library 42, the tester resource installation configuration 43, the program transfer rule check 44, the error codes list 45, the product target specification and the testing strategy 47.

Accordingly, the testing program of the present invention is provided by integrating the testing libraries, using and converting each testing specification of various testers so as to facilitate the development of the testing program, to reduce the time for developing the testing program and further to speed time to market for the product. The

present invention is file due to its patentability.

Many variations and modifications may be made by those skilled in the art without departing from the principles and spirit of the invention, the scope of which is defined by the appended claims.

WHAT IS CLAIMED IS:

1. An intellectual property of testers for automatically developing a testing program of a tester, comprising:

a tester library having testing program modules for plural testers, wherein said testing program modules are produced according to a testing strategy of said testers; and

an operation platform for automatically converting and producing said testing program of said tester in response to a testing requirement of said tester and according to said testing strategy of said tester library.

2. The intellectual property of testers for automatically developing a testing program of a tester according to claim 1, wherein said tester comprises a digital tester.

3. The intellectual property of testers for automatically developing a testing program of a tester according to claim 1, wherein said tester comprises an analog tester.

4. The intellectual property of testers for automatically developing a testing program of a tester according to claim 1, wherein said tester comprises a Trillium tester, a Schlumberger ITS serier tester, an HP 9491 tester, an Advantester T7315 tester and a VTT V7100 tester.

5. The intellectual property of testers for automatically developing a testing program of a tester according to claim 1, wherein said testing strategy comprises a testing item of a logic product and a testing item of an analog product.

6. The intellectual property of testers for automatically developing a testing program of a tester according to claim 5, wherein said testing item of said logical product is one selected from a group consisting of continuity test, drive/sink current test, power dissipation test, IDDQ test,

input leakage current test, function pattern test and AC characteristic test.

7. The intellectual property of testers for automatically developing a testing program of a tester according to claim 5, wherein said testing item of said analog product is one selected from a group consisting of ADC/DAC's SNR test, THD test, Jitter/Skew test, crosstalk test, eye diagram test and frequency response test.

8. A method for automatically developing a testing program of a tester, including following steps of:

establishing a testing program module for plural testers, wherein said testing program module comprises a testing strategy for said plural testers; and

automatically converting and producing a testing program source code prototype of said tester according to a testing requirement and said testing strategy.

9. The method for automatically developing a testing program of a tester according to claim 8, wherein said tester comprises a digital tester.

10. The method for automatically developing a testing program of a tester according to claim 8, wherein said tester comprises an analog tester.

11. The method for automatically developing a testing program of a tester according to claim 8, wherein said tester comprises a Trillium tester, a Schlumberger ITS serier tester, an HP 9491 tester, an Advantester T7315 tester and a VTT V7100 tester.

12. The method for automatically developing a testing program of a tester according to claim 8, wherein said testing strategy comprises a testing item of a logic product and a testing item of an analog product.

13. T The method for automatically developing a testing program of a

tester according to claim 12, wherein said testing item of said logical product is one selected from a group consisting of continuity test, drive/sink current test, power dissipation test, IDDQ test, input leakage current test, function pattern test and AC characteristic test.

14. The method for automatically developing a testing program of a tester according to claim 12, wherein said testing item of said analog product is one selected from a group consisting of ADC/DAC's SNR test, THD test, Jitter/Skew test, crosstalk test, eye diagram test and frequency response test.

INTELLECTUAL PROPERTY AND METHOD FOR DEVELOPING TESTING PROGRAM OF TESTER

ABSTRACT OF THE DISCLOSURE

An intellectual property of testers for automatically developing a testing program of a tester of the present invention includes a tester library having testing program modules for plural testers, wherein the testing program modules are produced according to a testing strategy of the testers; and an operation platform for automatically converting and producing the testing program of the tester in response to a testing requirement of the tester and according to the testing strategy of the tester library.

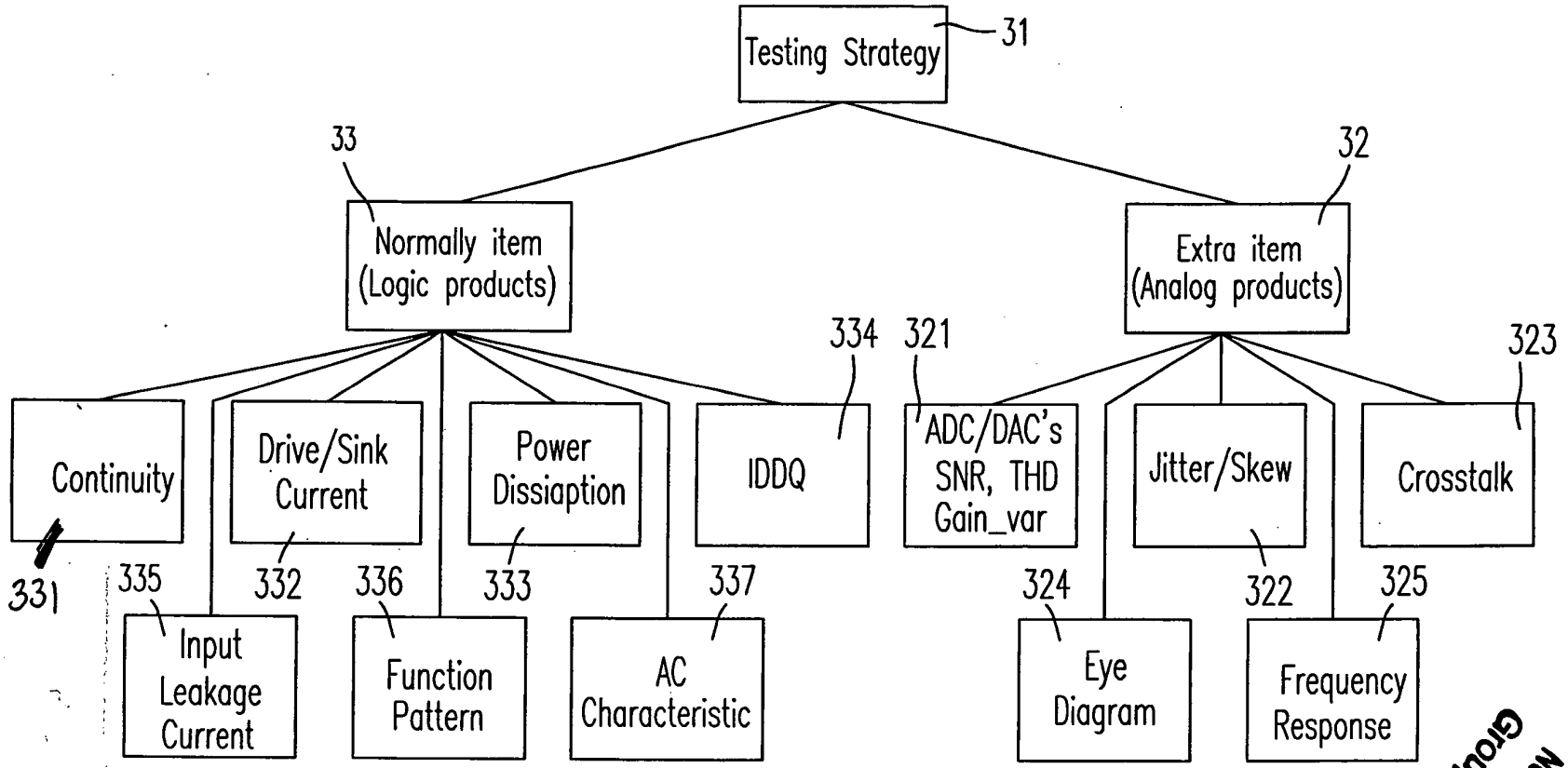

Fig. 3

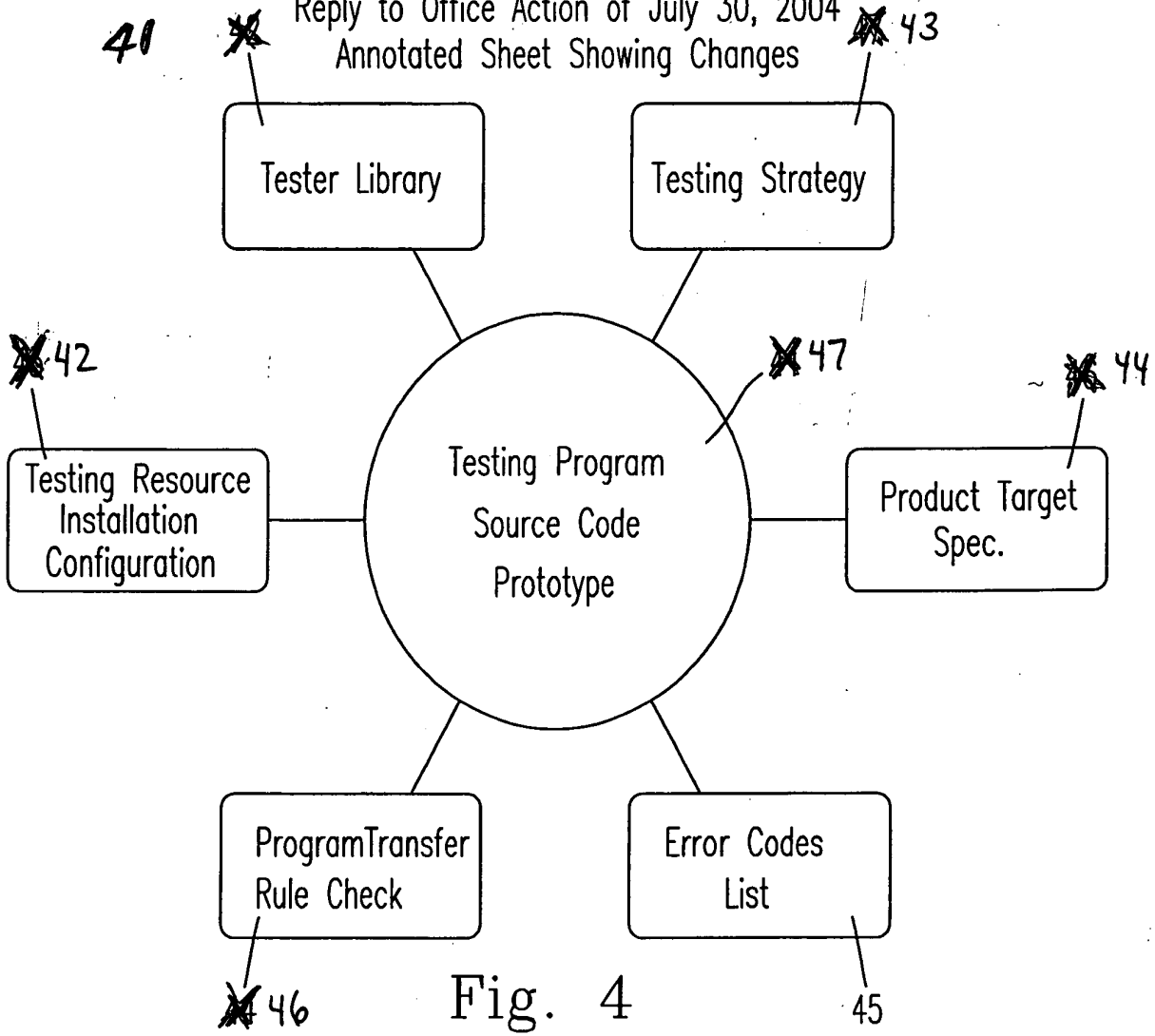

Fig. 4